UNITED STATES SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, WERNER BAUER, a citizen of Germany, residing at Bischwinder Str. 11, D-97497 Dingolshausen, Germany have invented certain new and useful improvements in a

WIRELESS DIGITAL DATA-TRANSMISSION PATH

of which the following is a specification.

BACKGROUND OF THE INVENTION

CROSS REFERENCE TO RELATED APPLICATIONS

Applicant claims priority under 35 U.S.C. §119 of German Application No. 100 39 187.7 filed August 10, 2000.

1. Field of the Invention

The present invention relates to a digital data-transmission path, particularly for the transmission of digital audio data, with a transmitter which receives a digital data stream to be transmitted, and a receiver for receiving the transmitted digital data stream.

2. The Prior Art

In the past, this digital data-transmission path has been used, for example, to transmit the stereo signals from a source such as a CD player wirelessly to a headset. A disadvantage of prior-art data-transmission paths of this kind is that they do not permit a 1:1 data transmission, or in other words a high-loss data transmission. In this connection, data-reduction algorithms are used among other techniques in order to ensure operation in the available megahertz transmission region. Thus the known transmission

paths have not been used for high-quality data transmission between, for example, a CD player and active speakers.

A further disadvantage of conventional digital data-transmission paths of the type cited above is that, due to limited bandwidth, they are restricted to the transmission of analog signals from the original two channels. In order to overcome the disadvantage of lossy data transmission, operation with more complex components have been designed, but these efforts have not been successful, because the associated costs are too high.

When analogue signals are transmitted by hardwire, multi-core arrangements are known in which, for example, analog signals are transmitted from a stage via microphones to a distant station, such as a recording and transmitting truck. This method of transmission of analog signals is subject to losses because the paths are relatively long, and must be spanned by cables. It is also costly, among other reasons because of the necessary local work for laying multicore cables.

An object of the present invention is to provide a digital data-transmission path which provides loss-free transmission of a digital data stream in an inexpensive

design, in order to overcome the disadvantages of the prior art.

A further object of the present invention is to replace prior art multi-core arrangements inexpensively for loss-free signal transmission.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a signal-processing circuit which subjects the digital data stream to be transmitted to signal-shape conversion so that the converted digital data stream can be transmitted without problems, or in other words, loss-free by the transmitter. This data stream can be received without problems by the receiver, and then processed by the receiver arrangement. According to an advantageous alternative version, however, the original digital data stream is recovered at the receiving end providing a signal-processing circuit complementary to the transmitter arrangement in the receiver arrangement, in order to recover the original signal shape of this data stream in a 1:1 correspondence.

The inventive signal-processing circuit(s) can be achieved extremely inexpensively with conventional components so that the digital data-transmission path can be processed

cost-effectively, since in all other respects it can also be based on a conventional cost-effective transmitter and a conventional cost-effective receiver.

The transmission frequency needed for the loss-free digital data transmission can be in the megahertz region. In order to make the data transmission and reception even more inherently immune from interference, the transmission frequency is selected in the gigahertz region. The gigahertz region has the added advantage that a much larger usable bandwidth is available, and therefore an even larger data stream can be transmitted than in the megahertz region.

The invention thus provides a loss-free data transmission with an inexpensive embodiment has not been possible heretofore because the signal shape of the digital data stream to be transmitted could not be processed loss-free by the transmitter (and by the receiver). Because the amplitude of the digital data stream was not optimally adapted to the transmitter (and receiver), and because in particular, the shape of the signal of the digital data stream, or in other words the pulse edges, were not adapted to the conditions of the transmitter. This disadvantage is overcome by the inventive signal-processing circuit in the transmitter arrangement. Moreover, due to the loss-free data

transmission, the inventive transmission path is suitable for high-quality wireless transmissions of audio signals, for example to active speakers.

According to a particularly advantageous improvement of the invention, more than the two audio channels that have been transmittable heretofore can also be transmitted by the inventive digital data-transmission path, so that this transmission path represents an inexpensive and reliable, loss-free replacement for prior-art multiplex applications. A preferred embodiment of the digital transmission path both with regard to a transmitter and receiver arrangement, specifically using conventional components are available in an integrated and thus miniaturized space-saving form at low cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and features of the present invention will become apparent from the following detailed description considered in connection with the accompanying drawings. It should be understood, however, that the drawings are designed for the purpose of illustration only and not as a definition of the limits of the invention.

In the drawing, wherein similar reference characters denote similar elements throughout the several views:

FIG. 1 shows the transmitter arrangement of a preferred two-channel digital audio transmission path; and

Fig. 2 shows the receiver arrangement of the preferred two-channel digital audio transmission path.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Turning now in detail to the drawings, the embodiment of a wireless digital data-transmission path shown in Figs. 1 and 2 is designed as a two-channel transmission path, for example for the transmission of digital audio data. This digital transmission path is not limited to two channels, however, but it can be expanded without difficulty to 384 channels, for example, using currently available circuitry. Alternatively, the data can also be transmitted in an "unformatted" form, or in other words not organized in channels.

Referring to FIG. 1, the transmitter-end arrangement of the digital data-transmission path includes on the input side, an analog-to-digital converter (hereinafter A/D converter) 10 and on the output side a transmitter 11 for transmission of digital data. In order to transmit from

transmitter 11, the full information content, the digital data stream at the output by A/D converter 10, to the receiver arrangement of Fig. 2, a signal-processing stage 12 is disposed between A/D converter 10 and transmitter 11, in order to condition the data stream output by A/D converter 10 so as to provide a loss-free data transmission to the receiver by means of transmitter 11.

A/D converter 10, is preferably a converter with a resolution of at least 24 bits, and a sampling frequency of at least 96 kilohertz, and used as a two-channel A/D converter. A/D converter 10 has two inputs 13 and 14 for receiving analog (stereo) signals. At output 15 of A/D converter 10, there is present a digital data stream, which constitutes a digital representation of the analog signals originally provided to inputs 13, 14 and which for example exists in S/PDIF format. Clock signals of the converter are present at two further outputs 16, 17 of A/D converter 10. In particular, a WLCK signal (where WLCK stands for word clock) is present at output 16, while an LRCK signal (where LRCK stands for left right clock) is present at output 17. The S/PDIF signal or the data stream at output 15 is characterized by a trapezoidal signal shape, and an amplitude of typically 0.5 volt. At least when transmitter 11 (and the corresponding receiver) is operated with a frequency in the

gigahertz region (or alternatively in the MHz region) in order to ensure an adequate bandwidth for transmission of the digital data stream, it has been found that this signal shape cannot be processed and radiated loss-free via transmitter 11, and received loss-free by the receiver. In order to overcome this shortcoming, signal-processing circuit 12, is used and has as its input stage, a buffer circuit 18, which receives from inverter stage 24, the S/PDIF signal from output 15 of A/D converter 10. Buffer circuit 18 has five parallel-connected inverter stages 19 to 23. At the output side of inverter stage 24 is connected a quartz oscillator 25 to ground. The feedback effect of signal-processing circuit 12 on the A/D converter is suppressed by buffer circuit 18. Preferably, buffer circuit 18 has six inverter stages of an integrated hex inverter.

The output of buffer circuit 18 is followed in processing circuit 12 by an amplitude-processing circuit 26 in the form of a flip-flop circuit, or a dual flip-flop. The digital data stream at the output of buffer circuit 18 is injected into the D input of a first flip-flop 27 and into the D input of a second flip-flop 28. The clock inputs of two flip-flops 27 and 28 are connected to clock output 17 of A/D converter 10, which supplies the LRCK pulse. At the Q outputs of two flip-flops 27 and 28 there is provided the

digital data stream that is present at the output of circuit 18, with an amplitude raised to TTL or HC level, namely to an amplitude of 3 volt. This data stream is injected into a NAND gate circuit 29.

NAND gate circuit 29 comprises four NAND gates 30, 31, 32 and 33. The two inputs of NAND gate 30 are connected in common to output 17 of A/D converter 10 and thus receive the LRCK pulse. Moreover, the two inputs of NAND gate 30 are connected to ground via a resistor 34. The output of NAND gate 30 is connected to one input of NAND gate 31, whose other input is connected to the Q output of flip-flop 28. The output of NAND gate 31 is connected to one input of NAND gate 33, whose other input is connected to the output of NAND gate 32. One output of NAND gate 32 is connected to the Q output of flip-flop 27 and the other input of NAND gate 32 is connected to output 17 of A/D converter 10, which controls the LRCK pulse signal. The output of NAND gate 33 forms the output of NAND gate circuit 29. At the output thereof there is a digital data stream, whose edges are steep compared with the original data stream at output 15 of the A/D converter. In particular, the data stream at the output of NAND gate circuit 29 is rectangular, whereas the signal shape of the output signal of the A/D converter is trapezoidal, as indicated in the foregoing.

To NAND gate circuit 29 there is connected an inverter circuit 34 for serial output of the digital data stream from NAND gate circuit 29. Inverter circuit 34 is connected via a resistor 35 to the output of NAND gate circuit 29. Specifically, inverter circuit 34 comprises four EXOR gates 36, 37, 38 and 39. One input of EXOR gate 36 is connected to the output of NAND gate circuit 29 via resistor 35, and the other input of EXOR gate 36 is connected to clock output 16 of A/D converter 10, which supplies the WLCK pulse signal. The output of EXOR gate 36 is connected to the output of EXOR gate 38 and to the output of EXOR gate 39, in order to apply these outputs in common to the output of inverter circuit 34. The two inputs of EXOR gate 37 are at positive supply voltage (5DVDD) for inverter circuit 34, and the output of EXOR gate 37 is connected to two inputs of EXOR gate 38. The two inputs of EXOR gate 39 are at ground.

The inverter circuit is followed by an output stage of buffer circuit 12 in the form of a buffer circuit 40, which is similar to buffer circuit 18, and has five buffer stages 41 to 45 connected in parallel. Buffer circuit 40 is connected on the input side to the output of inverter circuit 34, and on the output side to an amplitude-trimming circuit 46, which is connected on the output side to input 47 of transmitter 11. Amplitude-trimming circuit 46 comprises a

buffer stage 48, whose input and output are bridged by means of a resistor 49. Buffer stages 41 to 45 and 48 can be the six buffer stages of a hex inverter.

Because of processing circuit 12 connected upstream, transmitter 11 is accordingly supplied with a digital data stream whose signal shape, derived from the original data-signal stream of D/A converter 10, is designed with amplitude and edge steepness so that this data stream can be transmitted without problems, and loss-free, by transmitter 11.

Referring to FIG. 2, the receiver circuit has a receiver 50 with an antenna 51, which communicates wirelessly with an antenna 11a of transmitter 11. In an alternative embodiment, antennas 11a and 51 can be replaced by a fiber-optic transmission path.

Receiver 50 has on the output side a digital-to-analog converter (hereinafter D/A converter) 52, preferably with a resolution of at least 24 bits, and a sampling rate of at least 96 kHz. On the output side there are connected buffer/low-pass filter circuits 53 and 54, at the outputs of which there are present the recovered analog signals that were input into inputs 13 and 14 of A/D converter 10 in the

transmitter arrangement of Fig. 1. Between receiver 50 and D/A converter 52 there is connected a signal-processing circuit 55, which in its signal-shaping portions, represents the complement of signal-processing circuit 12 in the transmitter arrangement of Fig. 1, and which otherwise has upstream and downstream buffer circuits similar to those of the circuit arrangement of Fig. 1.

Output 155 of receiver 50 is followed by an amplitude-trimming circuit 56 in the form of a buffer stage 57, whose input and output are bridged with a resistor 58. To amplitude-trimming circuit 56 there is connected a buffer circuit 59, which comprises five buffer stages 60 to 64 connected in parallel.

Buffer circuit 59 is followed by a flip-flop circuit 65 for recovery of the original signal amplitude of the digital data stream at output 15 of the A/D converter at the level of about 0.5 volt. This flip-flop circuit comprises two flip-flops 66 and 67. The D input of flip-flop 66 and the D input of flip flop 67 are connected to the output of the buffer circuit. The clock input of flip-flop 66 and the clock input of flip-flop 67 are connected to a clock output 68 of D/A converter 52, which supplies an LRCK signal. The Q output of flip-flop 66 and the Q output of flip-flop 67 are connected

to a signal-processing circuit connected downstream from amplitude-processing circuit 65 and having the form of a NAND gate circuit 69, which comprises four NAND gates 70, 71, 72 and 73.

One input of NAND gate 70 is connected to the Q output of flip-flop 67. The other input of NAND gate 70 is connected to the output of NAND gate 71. The two inputs of NAND gate 71 are connected to ground (DGND). The output of NAND gate 70 is connected to one input of NAND gate 73. The other input of NAND gate 73 is connected to the output of NAND gate 72, whose one input is connected to the Q output of flip-flop 66, and whose other input is connected to clock output 68 of the D/A converter, which supplies the LRCK signal. The output of NAND gate 73 forms the output of NAND gate stage 69.

To NAND gate stage 69, which recovers the original edge steepness of the digital data stream at output 15 of A/D converter 10, there is connected an inverter circuit 74, which comprises four EXOR gates 75, 76, 77 and 78, and serves to output serially the data of the digital data stream from NAND gate circuit 69. One input of EXOR gate 75 is connected to its output and to one input of EXOR gate 76, while the other input of EXOR gate 75 is connected to the output of

NAND gate circuit 69 (output of NAND gate 73). The other input of EXOR gate 76 is connected to a clock output 89 of D/A converter 52, which supplies a WRCK signal, while the output of EXOR gate 76 is connected to both inputs of EXOR gate 77 and to the output of EXOR gate 78. The two inputs of EXOR gate 78 are at positive supply voltage of inverter circuit 74. The output of EXOR gate 77 forms the output of inverter circuit 74.

The output of inverter circuit 74 is connected to an amplitude-trimming circuit 79, which includes a buffer stage 80. The input and output are bridged by means of a resistor 81, which forms part of an integrated hex inverter, whose other five buffer stages 82 to 86 form the parallel-connected stages of a buffer circuit 87. Buffer circuit 87 is connected between amplitude-trimming stage 79 and data-stream input 88 of D/A converter 52. Thus, at the input 88, there is the recovered digital data stream corresponding to the data stream at output 15 of A/D converter 10. In the illustrated practical example, this is an S/PDIF data stream, which can be converted without problems into analog signals by D/A converter 52.

In the invention, the transmission frequency is preferably 2.465 GHz or in another mode would be preferably 868 MHz.

While only a single embodiment of the present invention have been shown and described, it is to be understood that many changes and modifications may be made thereunto without departing from the spirit and scope of the invention as defined in the appended claims.